

[Help](#) [FAQ](#) [Terms](#) [IEEE](#)[Quick Links](#)[»Table of Contents](#)[Peer Review](#)

Welcome to IEEE Xplore®

- ☐ Home
- ☐ What Can I Access?
- ☐ Log-out

Tables of Contents

- ☐ Journals & Magazines
- ☐ Conference Proceedings
- ☐ Standards

Search

- ☐ By Author
- ☐ Basic
- ☐ Advanced
- ☐ CrossRef

Member Services

- ☐ Join IEEE
- ☐ Establish IEEE Web Account
- ☐ Access the IEEE Member Digital Library

IEEE Enterprise

- ☐ Access the IEEE Enterprise File Cabinet

 Print Format**Computer-Aided Design of Integrated Circuits and Systems, IEEE Transactions on**

Volume: 22, Issue: 6, Year: June 2003

Guest Editorial*Hassoun, S.; Nowick, S.M.; Stok, L.*

Page(s): 662- 664

[\[Abstract\]](#) [\[PDF Full-Text \(216 KB\)\]](#)**Measurements for structural logic synthesis optimizations***Kudva, P.; Sullivan, A.; Dougherty, W.*

Page(s): 665- 674

[\[Abstract\]](#) [\[PDF Full-Text \(452 KB\)\]](#)**Timing-driven logic bi-decomposition***Cortadella, J.*

Page(s): 675- 685

[\[Abstract\]](#) [\[PDF Full-Text \(613 KB\)\]](#)**On the verification of sequential equivalence***Jiang, J.-H.R.; Brayton, R.K.*

Page(s): 686- 697

[\[Abstract\]](#) [\[PDF Full-Text \(837 KB\)\]](#)**A high-performance architecture and BDD-based synthesis methodology for packet classification***Prakash, A.; Kotla, R.; Mandal, T.; Aziz, A.*

Page(s): 698- 709

[\[Abstract\]](#) [\[PDF Full-Text \(474 KB\)\]](#)**Synthesis of reversible logic circuits***Shende, V.V.; Prasad, A.K.; Markov, I.L.; Hayes, J.P.*

Page(s): 710- 722

[\[Abstract\]](#) [\[PDF Full-Text \(685 KB\)\]](#)**PLA-based regular structures and their synthesis***Fan Mo; Brayton, R.*

Page(s): 723- 729

[\[Abstract\]](#) [\[PDF Full-Text \(596 KB\)\]](#)

Integrated floorplanning with buffer/channel insertion for bus-based designs

Rafiq, F.; Chrzanowska-Jeske, M.; Yang, H.H.; Jeske, M.; Sherwani, N.

Page(s): 730- 741

[\[Abstract\]](#) [\[PDF Full-Text \(692 KB\)\]](#)

Mixed-mode simulation approach to characterize the circuit delay sensitivity to implant dose variations

Srinivasaiah, H.C.; Bhat, N.

Page(s): 742- 747

[\[Abstract\]](#) [\[PDF Full-Text \(400 KB\)\]](#)

Lossy transmission line simulation based on closed-form triangle impulse responses

Tingdong Zhou; Dvorak, S.L.; Prince, J.L.

Page(s): 748- 755

[\[Abstract\]](#) [\[PDF Full-Text \(620 KB\)\]](#)

Modeling, testing, and analysis for delay defects and noise effects in deep submicron devices

Jing-Jia Liou; Krstic, A.; Yi-Ming Jiang; Kwang-Ting Cheng

Page(s): 756- 769

[\[Abstract\]](#) [\[PDF Full-Text \(638 KB\)\]](#)

Fault-coverage analysis techniques of crosstalk in chip interconnects

Yi Zhao; Dey, S.

Page(s): 770- 782

[\[Abstract\]](#) [\[PDF Full-Text \(689 KB\)\]](#)

Variable-length input Huffman coding for system-on-a-chip test

Gonciari, P.T.; Al-Hashimi, B.M.; Nicolici, N.

Page(s): 783- 796

[\[Abstract\]](#) [\[PDF Full-Text \(1048 KB\)\]](#)

An efficient test vector compression scheme using selective Huffman coding

Jas, A.; Ghosh-Dastidar, J.; Mom-Eng Ng; Toubia, N.A.

Page(s): 797- 806

[\[Abstract\]](#) [\[PDF Full-Text \(527 KB\)\]](#)

On the problem of gate assignment under different rise and fall delays

Oliveira, A.L.; Murgai, R.

Page(s): 807- 814

[\[Abstract\]](#) [\[PDF Full-Text \(509 KB\)\]](#)

1 2 [\[Next\]](#)

[Home](#) | [Log-out](#) | [Journals](#) | [Conference Proceedings](#) | [Standards](#) | [Search by Author](#) | [Basic Search](#) |
[Advanced Search](#) | [Join IEEE](#) | [Web Account](#) | [New this week](#) | [OPAC Linking Information](#) | [Your Feedbac](#)
[Technical Support](#) | [Email Alerting](#) | [No Robots Please](#) | [Release Notes](#) | [IEEE Online Publications](#) | [Help](#)
[FAQ](#) | [Terms](#) | [Back to Top](#)

Copyright © 2004 IEEE — All rights reserved